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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,522	02/06/2004	Herb H. Huang	021653-000900US	6545

20350 7590 08/18/2006

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EXAMINER	
RICHARDS, N DREW	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 08/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,522	HUANG ET AL.	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/15/06 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiau (US Patent No. 6,372,580 B1) in view of Yang et al. (US Patent No. 6,847,087 B2)

Shiau teach a method for manufacturing ROM memory devices in figure 4 and figures 5A-11D, the method comprising:

- forming a cell region as an array region for ROM memory devices (figure 4), the array including containing continuous bit line regions BN+ in each cell (the bit lines BN+ are formed in figures 6A-6D);

- forming a gate structure POLY within the cell region (figures 9A-9D);
- forming a first sidewall spacer 47 overlying a first side of the gate structure POLY and a second sidewall spacer 47 overlying a second side of the gate structure POLY (figures 10B and 10D, column 4 lines 47-48), each sidewall spacer extends over and overlaps a portion of source/drain regions BN+ (as in the instant application, the source/drain regions are a part of the bit lines BN+), the first and second sidewall spacer 47 also adapted to separate the gate structure POLY from the source/drain regions BN+;
- applying a refractory metal overlying the entire substrate including the gate structure POLY including the first and second sidewall spacers 47 (column 4 line 56 through column 5 line 4);
- heat treating to form silicide regions 51 overlying the gate structure POLY and exposed portions of the source/drain regions BN^+ (it is noted that Shiau does not explicitly state their heat treatment resulting in "alloying" the refractory metal; nonetheless, this is implicitly taught by Shiau as alloying is inherent in heat treating to form the silicide; that is, the silicon and the metal inherently alloy together in forming the silicide)
- and selectively removing the refractory metal layer from the sidewall spacers (figures 11A-11D and column 4 line 56 through column 5 line 4; note that the refractory metal layer is removed from all sections where it did not form an alloy, that is all section except for where the refractory metal contacted the polysilicon gate and silicon substrate directly).

Shiau does not teach forming a trench isolation structure within a cell region of the substrate. Since Shiau does not teach forming the isolation structure, Shiau also does not teach the claimed features and arrangement of the isolation structure and it's structural arrangement.

Yang et al. teach in figures 2(a)-2(c) a ROM memory array which includes continuous bit lines (SPW1/SPW2/SPW3) and gate structures (M0~M15) extending over and perpendicular to the bit lines. Yang et al. also teach a shallow trench isolation structure (STI) within a cell region. The shallow trench isolation structure, as seen in figures 2(b) and 2(c), are provided between adjacent bit lines extending in the same direction as the bit lines to isolate adjacent bit lines

Shiau and Yang et al. are from the same field of endeavor. At the time of the invention, it would have been obvious to one of ordinary skill in the art to employ the trench isolation structures of Yang et al. in the method and device of Shiau. The motivation for doing so is to isolate the bit lines from each other (Yang et al. column 4 lines 44-47). Therefore, it would have been obvious to combine Shiau with Yang et al. to obtain the invention of claim 1.

In combining the trench isolation regions of Yang et al. into the method and device of Shiau, the resulting method renders claim 1 obvious. In the combination, the trench isolation structure will separate a continuous bit line region of the cell from another bit line region from another cell, the sidewall spacers will extend over and overlap a portion of the trench isolation structure, and the trench isolation structure will

be separated from the gate structure by the sidewall spacers. Further, since the refractory metal layer of Shiau is applied over the entire substrate surface, it will be applied over an exposed portion of the trench isolation structure and the refractory metal will be selectively removed from the exposed surface of the trench isolation structure since it will not alloy to form the silicide on this portion.

With regard to claim 2, the refractory metal layer of Shiau is titanium or cobalt (column 4 line 56).

With regard to claim 3, the trench isolation region of Yang et al. is an STI region (figure 2(b)).

With regard to claim 4, it is obvious to one or ordinary skill in the art at the time of the invention that the STI region comprises silicon dioxide since silicon dioxide is a commonly used material for filling trenches in STI applications.

With regard to claim 6, the first and second sidewall spacers of Shiau are a dielectric material (column 4 line 52).

With regard to claim 7, the buried bit line structure of Shiau is within the source/drain region.

With regard to claim 8, the trench isolation STI is within the substrate at a predetermined depth which is greater than a junction depth of the buried bit line SPW (Yang et al., column 4 lines 48-51).

4. Claims 5 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiau with Yang et al. as applied to claims 1-4 and 6-8 above, and further in view of Iwata et al. (US 2004/0262650 A1).

Liu with Shiau do not explicitly disclose a channel region using a length of about 0.25 micron and less or the gate structure having a width of 0.25 micron and less. Iwata et al. teach semiconductor devices. Iwata et al. teach in paragraph 3 that recently the integration level of semiconductor devices is becoming higher and higher and thus there is a demand for smaller elements. Iwata et al. teach in paragraph 24 that the gate electrode (gate structure) is formed to a width of 100 nm (0.1 micron). It is noted that this paragraph relates to figure 44, which shows that channel length as the same as the gate width, thus Iwata teach both the gate structure and channel length of less than 0.25 micron.

Shiau with Yang et al. and Iwata et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to one of ordinary skill in the art to form the gate structure width and channel length to 0.25 micron or less. The motivation for doing so is to meet the demand for smaller elements for higher integration. Therefore, it would have been obvious to combine Shiau and Yang et al. with Iwata et al. to obtain the invention of claims 5 and 9.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shiau with Yang et al. as applied to claims 1-4 and 6-8 above, and further in view of Chang (US Patent No. 5,506,160).

Shiau and Yang et al. each teach an array of ROM cells (see figure 3A of Liu and figure 4 of Shiau, for example) but do not explicitly disclose their array having at least eight cells by eight cells. Nonetheless, it is considered obvious to form a ROM array to have at least eight cells by eight cells. Each cell represents one bit of data. Chang teach a ROM array in figure 5, for example. Chang et al. teach forming the array to be a 64 Mbit array. As one of ordinary skill in the art would recognize, a 64 Mbit array has at least eight cells by eight cells. At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the array of Shiau with Yang et al. to have at least eight cells by eight cells. The motivation for doing so is to meet an industry need of higher integration and larger memory arrays and to provide a greater amount of memory needed for modern electronics devices. Thus, it would have been obvious to form the array to at least eight cells by eight cells as claimed.

Response to Arguments

6. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

N. DREW RICHARDS
PRIMARY EXAMINER